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10ES32

# Third Semester B.E. Degree Examination, June 2012
## Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

**Note:** ***1. Answer FIVE full questions, selecting at least TWO questions from each part.***
***2. Missing data may be assumed suitably.***
***3. Draw equivalent circuit wherever necessary.***

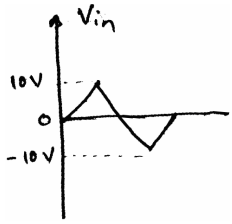
Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

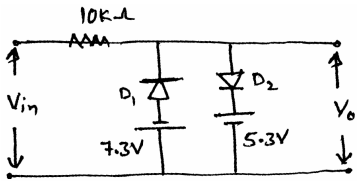
## PART – A

**1** a. Define :
i) Transition capacitance ; ii) Diffusion capacitance ; iii) Reverse recovery time. **(06 Marks)**

b. For the circuit shown in Fig.Q.1(b), sketch the output waveform and transfer characteristics for cut-in voltage = 0.7 V. **(08 Marks)**

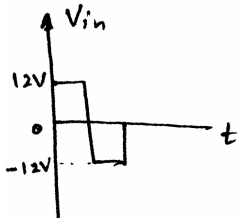
Fig.Q.1(b)

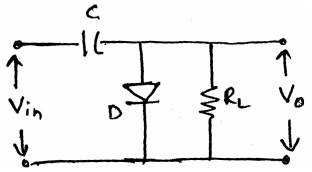



c. Sketch the output voltage waveform for the circuit shown in the Fig.Q.1(c). Assume Si = 0.7 V. **(06 Marks)**

Fig.Q.1(c)

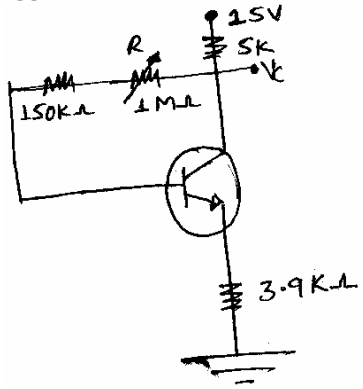



**2** a. Determine the levels of $I_{CQ}$ and $V_{CEQ}$ for the voltage divider configuration using the EXACT and APPROXIMATE techniques. Use $V_{CC}$ = 18 V, $R_1$ = 82 kΩ, $R_2$ = 22 kΩ, $R_C$ = 5.6 kΩ, $R_E$ = 1.2 kΩ, β = 50. **(08 Marks)**

b. For the circuit shown in Fig.Q.2(b), determine the range of possible values of $V_C$. Assume silicon transistor with β = 200, $V_{CC}$ = 15V. **(06 Marks)**

Fig.Q.2(b)

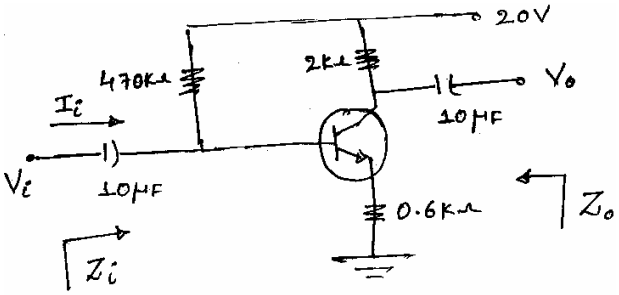



c. Derive an expression for the stability factor S(β) for a collector feedback bias circuit with $R_E$ = 0Ω. **(06 Marks)**

**3** a. Derive the expression for $A_v$, $A_i$, $Z_i$ and $Z_o$ of a voltage divider bias circuit using $r_e$ model. **(10 Marks)**

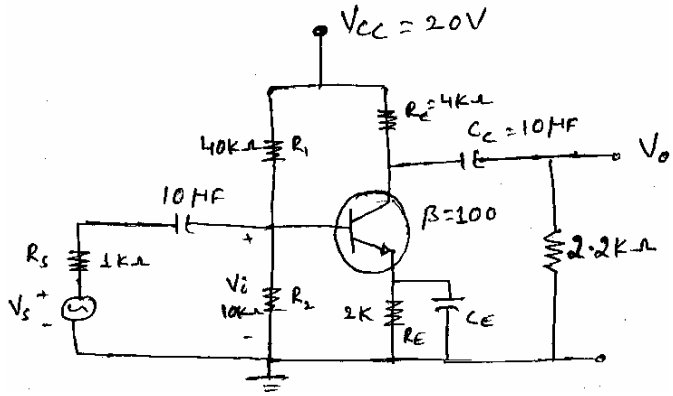
b. For the circuit shown in Fig.Q.3(b), calculate $r_e$, $z_i$, $z_o$, $A_V$, $A_I$, β = 120, $r_o$ = 40 kΩ for un bypassed ($R_E$). **(10 Marks)**

Fig.Q.3(b)




**4** a. Use the network shown in Fig.Q.4(a). i) Determine $f_{H_i}$ and $f_{H_o}$; ii) Find $F_{(B)}$ and $F_T$.

Fig.Q.4(a)




Take $C_\pi(c_{bc})$ = 36 pF, $Cu(c_{bc})$ = 4 pF, $C_{cc}$ = 1 pF, $C_{wi}$ = 6 pF, $C_{wo}$ = 8 pF, $r_o = \infty\Omega$. **(12 Marks)**

b. Define $f_\alpha$, $f_\beta$ and $f_T$ and state the relation between $f_\beta$ and $f_T$. **(08 Marks)**

## PART – B

**5** a. Obtain the expression for $Z_{in}$, $Z_o$ and $A_v$ for a Darlington Emitter follower. List the advantages of Darlington Emitter follower. **(10 Marks)**

b. List the general characteristics of negative feedback amplifiers. **(04 Marks)**

c. Determine the voltage gain, input and output impedance with feedback for voltage series having A = -100, $R_i$ = 10 kΩ and $R_o$ = 20 kΩ for feedback β = -0.1. **(06 Marks)**

**6** a. Explain with a neat sketches, how power amplifiers are classified. **(08 Marks)**

b. With a neat circuit diagram, explain the working of a complementary symmetry class B amplifier. **(08 Marks)**

c. Calculate the 2nd harmonic distortion for an O/P waveform displayed on an oscilloscope provides the following measurements : $V_{CE\ Min}$ = 1V, $V_{CE\ Max}$ = 22V, $V_{CEQ}$ = 12V. **(04 Marks)**

**7** a. What is Barkhausen criterion? Explain how oscillations start in an oscillator. **(06 Marks)**

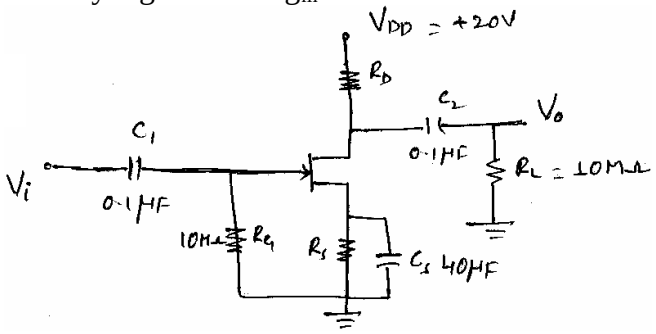
b. Differentiate between RC phase shift oscillator and Wein Bridge oscillator. **(06 Marks)**

c. Explain with a neat circuit diagram of a Hartley oscillator. Write the expression for the frequency of oscillations. **(08 Marks)**

**8** a. With necessary equivalent circuit obtain the expression for $Z_i$ and $A_V$ for a JFET common gate configuration. **(10 Marks)**

b. Design the values of $R_D$ and $R_S$ for the network shown in Fig.Q.8(b) that will result in a gain of 8 using a relatively high level of $g_m$ for this device defined at $V_{GSQ} = 1/4\ V_p$. **(10 Marks)**

Fig.Q.8(b)




$I_{DSS} = 10mA$, $V_p = -4V$ } $g_{mo} = 5ms$

$Y_{OS} = 20\mu s$

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